What is claimed is:

1. A method comprising:

receiving one or more bits of synchronization data in a receiver of a communications link;

loading the one or more bits of synchronization data into a shift register in the receiver, wherein the receiver shift register has a feedback circuit;

if the receiver shift register is filled with synchronization data, initiating synchronized operation of the receiver shift register with a corresponding transmitter shift register; and

if the receiver shift register is not filled with synchronization data, shifting the loaded synchronization data and loading one or more additional bits of synchronization data into the receiver shift register.

2. The method of claim 1, wherein receiving one or more bits of synchronization data comprises receiving idle codes containing synchronization data.

3. The method of claim 1, further comprising determining whether the receiver shift register is filled with synchronization data by counting a predetermined number of cycles after a reset event.

4. The method of claim 1, wherein the receiver shift register comprises a plurality of serially coupled flip-flops, and wherein shifting the loaded synchronization data comprises shifting the bit in each flip-flop to a next flip-flop.

5. The method of claim 1, wherein loading the one or more additional bits of synchronization data into the receiver shift register comprises loading the one or more additional bits of synchronization data into one or more predetermined cells of the receiver shift register.

6. The method of claim 1, wherein during synchronized operation, a bit sequence generated by the receiver shift register is compared to a received bit sequence to identify the occurrence of errors.

7. A system comprising:

a receiver shift register; and

a feedback circuit coupled to the receiver shift register;

wherein one or more cells of the receiver shift register are configured to alternatively accept as input either a bit from a preceding cell or a received bit of synchronization data.

8. The system of claim 7, further comprising a counter coupled to the shift register, wherein the counter is configured to assert a "synchronized" signal when a predetermined count is reached after a reset event.

9. The system of claim 8, wherein the predetermined count corresponds to the shift register being filled with synchronization data.

10. The system of claim 7, wherein the one or more cells of the shift register are configured to accept received bits of synchronization data as input until the shift register is filled with synchronization data, and to accept bits from preceding cells as input when the shift register is filled with synchronization data.

11. The system of claim 7, wherein upon occurrence of a reset event, data in the shift register is invalid data.

12. The system of claim 7, further comprising one or more demultiplexers coupled to provide input to the one or more cells, wherein the one or more demultiplexers are configured to select either bits from preceding cells or received bits of synchronization data to provide as input to the one or more cells.

13. The system of claim 12, wherein the demultiplexers are coupled to receive an indication of whether the receiver shift register is synchronized.

14. The system of claim 13, wherein the demultiplexers are coupled to a counter, wherein the counter is configured to provide the indication when a predetermined count is reached after a reset event.

15. The system of claim 7, further comprising a transmission medium coupled to the receiver shift register.

16. The system of claim 15, wherein the transmission medium is configured to transport the synchronization data in idle codes.

17. The system of claim 7, further comprising a transmitter shift register which is configured to generate a first bit sequence, wherein the receiver shift register is configured to generate an identical bit sequence.

18. The system of claim 7, wherein the feedback circuit is configured to generate a pseudorandom pattern.

19. The system of claim 7, wherein the receiver shift register is configured to load synchronization data on each cycle into one or more predetermined cells of the receiver shift register.

20. The system of claim 19, wherein the one or more predetermined cells of the receiver shift register exclude at least one of the cells of the receiver shift register.

21. The system of claim 20, wherein the receiver shift register cells comprise 11 serially coupled flip-flops and wherein the predetermined cells comprise 8 consecutive ones of the 11 serially coupled flip-flops.

22. The system of claim 7, wherein the feedback circuit comprises an exclusive OR (XOR) gate having two inputs coupled to receive the outputs of two of the cells of the receiver shift register, the XOR gate further having an output that is coupled to the input of a first cell of the receiver shift register.

23. A system comprising:

a receiver shift register; and

a feedback circuit coupled to the receiver shift register;

wherein one or more cells of the receiver shift register are configured to initially alternatively accept as input a received bit of synchronization data and, upon receiving an indication that the shift register is synchronized, accept as input a bit from a preceding cell.